IN THE CLAIMS

Please amend the claims as follows:

1-2. (canceled)

3. (previously presented) The method of reading a mark on a semiconductor wafer according to claim 26, wherein the second mark is reproduced by means of forming said second mark identical to the mark at a second location spaced apart from the first mark.

4. (previously presented) The method of reading a mark on a semiconductor wafer according to claim 26, wherein the first mark is reproduced by means of forming a second mark identical to the first mark at a second location in the vicinity of the first mark.

5. (previously presented) The method of reading a mark on a semiconductor wafer according to claim 26, wherein the second mark is formed by means of a combination of dots, each dot measuring 1 to 13 μm wide, and the first mark is reproduced by means of forming a second mark identical to the first mark at a second location in the vicinity of the first mark.

6. (previously presented) The method of reading a mark on a semiconductor wafer according to claim 26, wherein the second mark is a minute ID mark which is assigned to the semiconductor wafer and is formed by means of a combination of dots, each dot measuring 1 to 13 μm wide, and the first mark is reproduced by means of forming a second mark identical to the first mark at a second location in the vicinity of the first mark.

7-12. (canceled)

13. (previously presented) The method of claim 26 further including the step of providing said first ad second marks at positions where the marks are to undergo the same surface treatment at different speeds during the course of manufacture.

14. (previously presented) The method of claim 26 further including the step of providing said first and second marks on the front side of the semiconductor wafer and a third mark on the reverse side of said semiconductor wafer, such that the first, second and third marks undergo the same surface treatment at different speeds during the course of manufacture.

15. (previously presented) The method of claim 26 further including the step of providing said first and second marks on the front side of the semiconductor wafer and a third

mark on the reverse side of said semiconductor wafer, such that the first, second and third marks are located close to each other and such that the first, second and third marks undergo the same surface treatment at different speeds during the course of manufacture.

16. (previously presented) The method of claim 26 further including the step of providing said first and second marks on the front side of the semiconductor wafer and a third mark on the reverse side of said semiconductor wafer, such that the first, second and third marks under go the same surface treatment at different speeds during the course of manufacture and such that the first, second and third marks are located within an area where a single optical reading machine can read the first, second and third marks simultaneously.

17. (previously presented) The method of claim 26 further including the step of forming the first and second marks by means of a combination of dots, each dot measuring 1 to 13 μm wide, and providing said first and second marks on the front side of the semiconductor wafer and a third mark is provided on the reverse side of said semiconductor wafer, such that the first, second and third marks undergo the same surface treatment at different speeds during the course of manufacture and such that the first, second and third marks are located within an area where a single optical reading machine can read the first, second and third marks simultaneously.

18. (previously presented) The method of claim 26 further including the step of assigning said first and second marks ID marks to the semiconductor wafer as a combination of dots, each dot measuring 1 to 13 μm wide, providing said first mark on the front side of the semiconductor wafer and said third mark identical to said first and second marks on the reverse side of said semiconductor wafer, such that the first, second and third marks undergo the same surface treatment at different speeds during the course of manufacture and such that the first, second and third marks are located within an area where a single optical reading machine can read the first, second and third marks simultaneously.

19. (previously presented) The method of claim 26 further including the step of assigning ID marks to said first and second marks to the semiconductor wafer, and forming said ID marks by a combination of dots, each dot measuring 1 to 13 μm, affixing said ID marks on the interior wall surface of a notch, and providing said first mark on the front side of the semiconductor wafer and a third mark identical to said first and second marks on the reverse side

of said semiconductor wafer, such that the first, second and third marks undergo the same surface treatment at different speeds during the course of manufacture and such that the first, second and third marks are located within an area where a single optical reading machine can read the first, second and third marks simultaneously.

20. (previously presented) The method of claim 26 further including the steps of forming said first and second marks by means of a combination of dots, each dot measuring 1 to 13 μm for positioning purpose, and providing said first and second marks on the front side of the semiconductor wafer and a third mark identical to said first and second mark on the reverse side of said semiconductor wafer, such that the first, second and third marks undergo the same surface treatment at different speeds during the course of manufacture and such that the first, second and third marks are located within an area where a single optical reading machine can read the first, second and third marks simultaneously.

21. (previously presented) The method of claim 26 further including the steps of forming first and second marks by means of a combination of dots, each dot measuring 1 to 13 μm and indicating a crystal orientation of the semiconductor wafer, and providing said first and second marks on the front side of the semiconductor wafer and a third mark identical to said first and second marks on the reverse side of said semiconductor wafer, such that the first, second and third marks undergo the same surface treatment at different speeds during the course of manufacture and such that the first, second and third marks are located within an area where a single optical reading machine can read the first, second and third marks simultaneously.

22. (previously presented) The method of claim 26, wherein the semiconductor wafer is perfectly annular; and including the steps of forming first and second identical marks by means of a combination of dots, each dot measuring 1 to 13 μm and indicating crystal orientation of the semiconductor wafer; and providing said first and second mark on the front side of the semiconductor wafer and providing a third mark identical to said first and second marks on the reverse side of said semiconductor wafer, such that the first, second and third marks undergo the same surface treatment at different speeds during the course of manufacture and such that the first, second and third marks are located within an area where a single optical reading machine can read the first, second and third marks simultaneously.

23. (previously presented) The method of claim 26 further including the steps of aligning said first and second marks in a single direction; and providing said first and second marks on the front side of the semiconductor wafer and providing a third mark identical to said first and second marks on the reverse side of said semiconductor wafer, such that the first, second and third marks undergo the same surface treatment at different speeds during the course of manufacture and such that the first, second and third marks are located within an area where a single optical reading machine can read the first, second and third marks simultaneously.

24-25. (canceled)

26. (currently amended) A method of reading a mark on a semiconductor wafer, comprising the steps of:

forming a first mark capable of identifying said wafer, said first mark being separate and distinct from a second mark, each of said first and second marks having an identical content and being in an identical format on an interior wall of a notch of each of a plurality of said semiconductor wafers;

storing the plurality of semiconductor wafers in a wafer carrier by aligning said notches; and

simultaneously reading the first and second marks on the interior wall of said notch by an optical reader.